THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Low k Interlevel Dielectric Layer Fabrication Methods

To:

Box RCE

Commissioner for Patents

P. O. Box 1450

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From:

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

This Request for Continued Examination (RCE) Application is being filed in an abundance of caution to ensure consideration of the references listed on the attached form PTO-1449.

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

Respectfully submitted,

Dated: 11 Mey 9005

Ву

James E Jake Reg. No. 44,854

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Form PTO-144	49		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. MI22-1398			SERIAL NO. 09/536,037		
OIPE		APPLICANT: Li et al.									
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U.S. PATENT: 000 UMENTS											
*Examiner's Initials		Document Number	Date	Name		Class	Subclass		Filing If App	g Date propriate	
	АА	6,121,133	09/19/00	lyer et al.	lyer et al.		636				
	АВ	6,632,712 B1	07/11/00	Ang et al.	Ang et al.		212				
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	AD										
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FOREIGN PAT	TENT DC	CUMENTS	<u></u>				<u></u>				
		Document	Date	Coun	ntry	Class	Sub	class	Transla	etion	
!		Number							Yes	No	
	AJ	TW 47112 A	01/01/2002	Taiwan – Abstract					x		
	AK										
	AL										
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)											
	АМ	Wolf, S., and Tauber, Richard, Silicon Processing for the VLSI Era; Vol. 1; P "Silicon: Single Crystal Growth and Wafer Preparation"; pages 1 and 2						ss Tecl	nnology;		
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.